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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,197	01/28/2004	Douglas L. Youngblood	INSL.0083	3357

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EXAMINER	
LAO, LUN YI	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/766,197	YOUNGBLOOD ET AL.	
	Examiner	Art Unit	
	LUN-YI LAO	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1--4 and 8-22* is/are rejected.

7)☒ Claim(s) *5-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/13/2004 and 5/12/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 5-8 are objected to because of the following informalities:

"Q" is undefined in claim 5.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 9-14 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yer et al(US 20020109655) in view of Tanaka et al(US 20030132906).

As to claims 1, 9-14 and 19-22, Yer et al teaches a gamma correction circuit comprising: a resistor ladder(see figure 3) coupled to a reference voltage(Vdd); a plurality of adjustable tap resistors(81b) distributed along the resistor ladder and providing a plurality of selectable tap voltages(see figures 1, 3; paragraphs 19-21, 63 and 68); a programmable non-volatile memory(81a, EEPROM) that stores at least one digital gamma value(see figure 9; paragraphs 63-69 and 72-73); select logic(for

selecting resistance value of the variable resistor(81b) based on the digital information stored in the memory(81a), coupled to the memory(EEPROM) and to the plurality of adjustable tap resistors(81a), that selects each of the selectable tap voltages according to the at least one digital gamma value(see figures 3, 9; paragraphs 68-69 and 72-73); and a plurality of buffers(37) having inputs receiving selected tap voltages and outputs that provide a plurality of gamma correction voltages(see figures 3, 8-9; paragraphs 16-21; 67-73).

Yer et al teach a multiple channel programmable gamma correction voltage generator, comprising: a reference voltage(Vdd) applied across a resistor ladder(see figures 1, 3; paragraphs 19-21, 63 and 68); the resistor ladder including M adjustable tap resistors(M could be 1-10) distributed along the resistor ladder, each providing a corresponding one of M tap voltages distributed according to a gamma correction value; M buffers(M could be 1-10, 37), each having an input receiving a corresponding one of the M tap voltages and an output providing a corresponding one of M gamma correction voltages; select logic that selects a tap point of each of the M adjustable tap resistors to select each of the M tap voltages based on corresponding select values(see figures 3, 9; paragraphs 68-69 and 72-73); and a programmable non-volatile memory device, coupled to said decoder logic, that provides said select values indicative of said gamma correction value(see figures 3, 8-9; paragraphs 16-21; 67-73).

Yer et al fail to disclose an integrated circuit.

Tanaka et al teach an integrated gamma correction circuit(see figures 1-3, 11 and paragraph 8). It would have been obvious to have modified Yer et al with the

teaching of Tanaka et al, so as to reduce the number of connecting wires, ensure more stable correction, minimize space and the number of parts in providing the display control circuitry.

As to claim 9, it would have been obvious to have a set of latches with an external load coupled to the memory device and providing the select values to the select logic since Yer has disclosed latches(52, 53) for temporally storing data(see figures 3, 5, 8-9 and paragraphs 27-30).

As to claim 10, Yer teaches memory device(81a) stores a plurality of sets of select values, each corresponding to a different gamma correction value, and wherein the memory device(81a) includes an address control input for selecting from among the plurality of sets of select values and loading the set of latches(see figures 5, 8-9; paragraphs 27-30 and 63-73).

As to claim 13, Yer teaches each of said M buffers(37)comprises an operational amplifier configured as a voltage follower(see figure 3 and paragraphs 16-18).

As to claim 21, Yer et al teach the imaging device comprises an LCD panel(see figure 1; abstract and paragraphs 5-6).

As to claim 22, Yer et al teach control logic(85) coupled the memory(81a) via address control, wherein the control logic(85) enables selection of a plurality of digital gamma values stored in the memory(81a)(see figures 8-9 and paragraphs 72-73).

4. Claims 2-4 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yer et al(US 20020109655) in view of Tanaka et al(US 20030132906) and Suzuki et al(6,157,335).

As to claims 2-4 and 15-18, Yer et al as modified fail to disclose an adjustable tap resistors having plurality of resistor coupled in series and forming a plurality of junctions and switch logic that selects one of said plurality of junctions.

Suzuki et al teach a circuit having an adjustable tap resistors(R3a-R3h) having plurality of resistor coupled in series and forming a plurality of junctions and switch logic that selects(SW1-SW8) one of the plurality of junctions(see figures 4, 8 and column 6, lines 20-58). It would have been obvious to have modified Yer et al as modified with the teaching of Suzuki et al, so as to easy and accurate to select different resistance values and output voltages values(see column 2, lines 26-41).

As to claims 2 and 16, Yer et al as modified by Suzuki et al teach a plurality of first resistors distributed along the resistor ladder, each coupled to a corresponding one of the plurality of adjustable tap resistors, each first resistor comprising: a plurality of second resistors(R3a-R3h), coupled in series forming a plurality of first junctions; and first switch logic(SW1-SW8) that inserts the corresponding one of the plurality of adjustable tap resistors at one of the plurality of first junctions(see Yer's figures 3, 8 and Suzuki's figures 4, 8 and column 6, lines 20-58).

As to claim 3, Suzuki et al teach select logic includes decoder logic(23) which closes one of the P-1(P is greater than 2) switches of each of the M(M is greater than 1) adjustable tap resistors to select each of the M tap voltages based on a

corresponding one of M select values from the memory device(see figures 4 and column 6, lines 26-53).

As to claim 4, Yer as modified by Suzuki teaches a decoder logic(23)comprises M decoders, each receiving a corresponding one of said M select values and selecting a corresponding one of the P-1(P is greater than 2) switches of a corresponding one of the M adjustable tap resistors(see figures 4 and column 6, lines 26-58).

As to claim 17, Yer et al as modified by Suzuki et al teach each of the plurality of adjustable tap resistors comprises: a plurality of third resistors coupled in series and forming a plurality of second junctions; and second switch logic that selects one of said plurality of second junctions; and the select logic providing a gross adjustment to each said first switch logic and a fine adjustment to each the second switch logic(see Yer's figures 3, 8 and Suzuki's figures 4, 8 and column 6, lines 20-58).

As to claim 18, it would have been obvious to have a set of latches coupled to the memory since Yer has disclosed latches(52, 53) for temporally storing data(see figures 3, 5, 8-9 and paragraphs 27-30). Yer teaches a method for enables programming and selection of a plurality of a plurality of digital gamma values in memory(81a); and control logic(85) providing address control to the memory(81a) for selecting one of said plurality of digital gamma values(see figures 5, 8-9; paragraphs 30 and 63-73).

Allowable Subject Matter

5. Claims 5-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Liaw et al(6,424,281) teaches a circuit having a programmable switch.

Woo et al(20020101416) teaches a programmable DAC.

Chang et al(20030142084) teach a gamma correction circuit.

Chen et al(20020158862) teach a gamma correction circuit.

Bu(20030122757) teaches a gamma correction circuit.

Chuang et al(20040233182) teach a gamma correction circuit.

Medina et al(6,359,389) teach a gamma correction circuit having variable resistances.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lun-yi Lao whose telephone number is 571-272-7671. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 30, 2007

L. Y. Lao

Lun-yi Lao
Primary Examiner